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MIPS I-Class I6400 Multiprocessor Core

The MIPS I6400 multiprocessor core brings the proven and respected MIPS64 architecture and a suite of key features and capabilities to a wide range of markets and applications.

The I6400 achieves superior performance/efficiency levels and incorporates compelling features such as simultaneous multi-threading (SMT), hardware virtualization, 128-bit SIMD, advanced power management, multi-context security, and extensibility to coherent multi-cluster operation.

High efficiency and unique feature set
The MIPS I6400 CPU is a ground-up design based on a compact 9-stage dual-issue pipeline and utilizing SMT to set a new standard for performance efficiency among CPU cores in its class. It is available as fully synthesizable RTL, allowing for a wide range of implementations in a single process node and across process geometries.

In TSMC 28HPM process technology, one fully configured I6400 base core1 fits in 1 mm2[1] and achieves 1 GHz (under worst case conditions and slow corner silicon) while delivering 3000 DMIPS and 5600 CoreMark[2].

The processor can approach 2 GHz with more aggressive implementations and operating conditions.

Better 64-bit computing
The I6400 is a full MIPS64 processor delivering a unique combination of small size with big performance, extending far beyond other 64-bit mid-range processor cores on the market. However, its flexibility and efficiency also enable it to be a compelling alternative against traditional 32-bit processor IP cores, and even challenging many higher end 64-bit core offerings – but in a fraction of the size and power.

But the performance and efficiency characteristics of the I6400 are just the beginning. The I6400 is the first core in the MIPS lineup based on Release 6, the latest release of the MIPS64 architecture.

Release 6 is essentially a streamlining of the MIPS architecture, driven by the goal of enhancing execution on more modern software workloads, including Just-In-Time compilers (JITs), Virtual Machines (VMs) and Position Independent Code (PIC). These technologies and constructs are commonly found in Android, Javascript, Browsers, and newer compiler technologies such as LLVM.

Furthermore, MIPS64 is a proper superset of the MIPS32 architecture. As such, MIPS64 can run MIPS32 software directly as well – no separate ISAs or mode switching is required.

Full hardware virtualization support
With support for hardware virtualization, the I6400 joins the P5600 and the M5100/M5150 cores to provide this key technology from top to bottom in the MIPS Warrior generation cores lineup. This feature enables more traditional uses of virtualization, such as multi-OS systems for Enterprise class applications, but also serves as the foundation for multi-context security solutions for IoT, wearables, consumer and mobile applications. The I6400 supports full hardware virtualization with Guest and Root privilege levels, allowing existing MIPS software and ecosystem to be run unaltered within Guest domains, with hypervisor/secure kernel control in Root privilege level.

An efficient 128-bit SIMD engine
This new processor core also features a dual-issue and multi-threaded FPU/SIMD unit, well suited for a wide variety of compute intensive tasks such as audio, vision, and video processing. The scalar and SIMD floating point functionality is fully IEEE-754 2008 compliant, and supports 8-/16-/32-/64-bit integer and fixed point data types, as well as 16-/32-/64-bit floating point data types.

The next step in heterogeneous computing
The I6400 was designed for use in multi-core applications. As a multi-core system, it includes integrated L2 cache and virtualized support for globalized interrupts and I/O coherency.

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A key step forward is a new coherence management scheme relative to previous MIPS multi-core products, moving from snoop-based to directory-based coherency and improving power consumption, performance, and scalability. The coherence manager (CM) can support up to six cores in a multi-core cluster, and each core in the cluster can run at its own clock and voltage level, supporting more heterogeneous operating environments and providing a whole new level of advanced power management. The new CM was also designed for extensibility into coherent multi-cluster implementations.

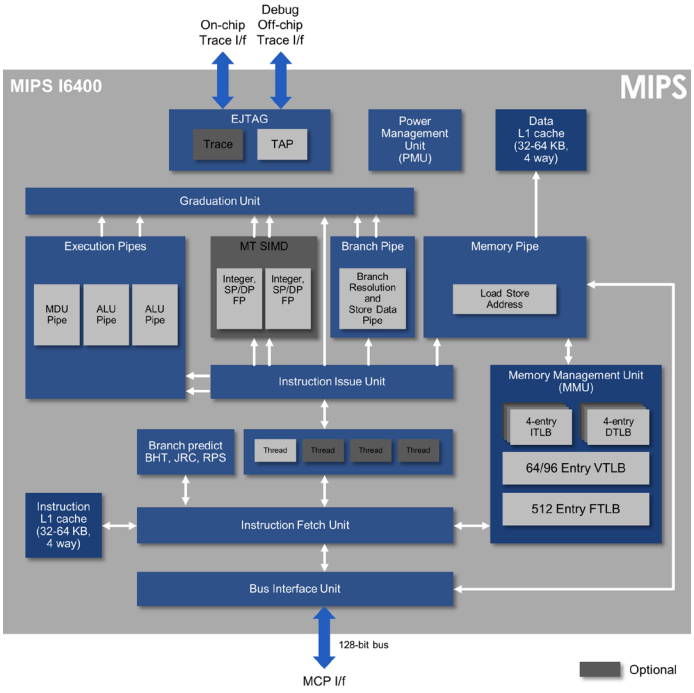
Given its robust performance in a small footprint, the MIPS64 architecture that also supports MIPS32 directly, and a plethora of compelling and differentiated new features, the I6400 is a CPU solution that addresses the needs of a very broad set of markets and applications. It can be used in many core systems with MT and virtualization and ECC running 64-bit software for enterprise-class solutions, all the way down to single or dual core implementations running an RTOS for deeply embedded apps – and many permutations and markets in between.

[1] Base core configuration is one of the cores in a multi-core cluster, and includes 32KB L1$s, full TLBs, MT FPU/SIMD unit, and virtualization support. It does NOT include coherence manager or L2$ or cluster level functionality. All specs and benchmark data indicated are preliminary.

[2] All specs and benchmark data indicated are preliminary. Worst case, slow corner conditions assume slow/slow corner silicon running at Vnom – 10%, Temp = 0C, and 8% OCV + 25ps clock jitter margin. More aggressive implementation and operating conditions as referenced could include higher performance libraries and memories, voltage overdrive, typical silicon and more relaxed operating specs.

I6400 Benefits

- Brings MIPS64 - a proven, successful, well supported 64-bit architecture – to a much broader set of customers as a licensable IP core.
- Delivers compelling performance/power/area form factors, flexibility and features well suited for broad range of markets and applications, from deeply embedded to automotive to consumer/mobile and all the way up to enterprise class storage/server/dataplane solutions.
- 128-bit SIMD - accelerates execution of audio, video, graphics, imaging, speech and other DSP-oriented software algorithms, with instruction set designed for development in high level languages such as C, OpenCL.
- MIPS multi-domain security technology – ensuring that applications that need to be secure are effectively and reliably isolated from each other, as well as protected from non-secure applications.
- Multiple context security platform for enterprise/consumer partitioning, secure content access, payments/transactions, and isolating secure schemes from numerous content sources.
- Broad software and ecosystem support and mature toolchain.
- Available as synthesizable IP, for implementation in any process node, with standard cells and memories.



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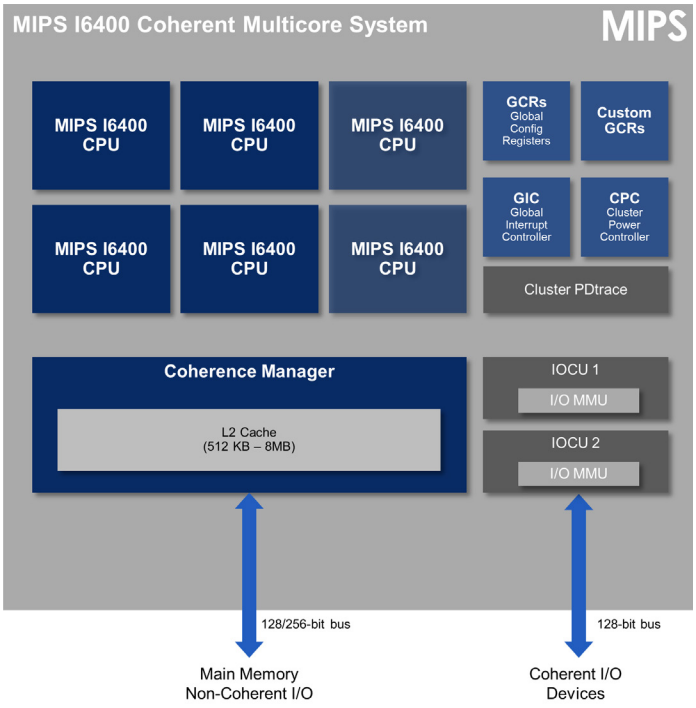
I6400 Base Core Features

- 64-bit MIPS64 Release 6 Instruction Set Architecture
  - Proven, successful, well supported 64-bit architecture
  - Superset of MIPS32 – runs MIPS32 software directly
- Balanced, 9-stage, dual-issue pipeline with Simultaneous Multi-Threading (SMT)
  - Superscalar on a single thread or two threads simultaneously per cycle
  - Up to 4 threads per core
  - Instruction bonding – merges sequential integer or floating point loads or stores into one operation for up to 2x increase on memory-intensive data movement routines
- New high-performance dual-issue FPU/SIMD Unit - optional
  - 32 x 128-bit register set, 128-bit loads/stores to/from SIMD unit
  - Native data types:
  - 8-/16-/32-/64-bit integer and fixed point, 16-/32-/64-bit floating point
  - IEEE-754 2008 compliant
- Full hardware virtualization
  - Provides root and guest privilege levels for kernel and user space
  - Supports multiple guests, with full virtual CPU per guest = guest OSs run unmodified
  - Separate TLBs, COP0 contexts for root and guests –> full isolation, fast context switching, exception and interrupt handling by root
  - Complete SoC virtualization support (IOMMU and interrupt handling – see multi-core features)
- L1 cache
  - Instruction and Data of 32KB or 64KB each with ECC, 4-way set associative
- Programmable Memory Management Unit (MMU)
  - 1st and 2nd level TLBs with arrays for variable and fixed page size support

Coherent Multi-Core Processor Features

- Complete multi-core system designed for maximum cluster-level bandwidth
  - Coherence manager
    - Supports multi-core configurations up to six cores in a single cluster
    - New directory-based coherency scheme – improves power consumption, performance and scalability
    - Extensibility to multi-cluster implementations
    - Multiple I/O coherency (IOCU) interfaces
  - Global interrupt controller (GIC) with 256-interrupts
  - High-bandwidth 256-bit internal data paths and external system interface
  - Integrated L2 cache (L2$): 16-way set associative, up to 8MB of memory
    - ECC option on L2$ RAM for higher data reliability
    - Configurable wait states to RAM for optimal L2$ design
    - L2$ hardware pre-fetch for higher throughput and performance
  - Advanced power management
    - Core-level DVFS (dynamic voltage and frequency scaling) – each core can be run independently at it's own clock and voltage level
  - Virtualization support at system and SoC level
    - IOCUs include I/O MMU, GIC has virtualized interrupts
    - Guest ID brought out on system i/f for integration into virtualized SoC design
- Advanced debug capabilities – PDtrace subsystem allows visibility to core- and cluster-level trace information



About Wave Computing

Wave Computing, Inc. is revolutionizing AI with its dataflow-based systems and solutions that deliver orders of magnitude performance improvements over legacy architectures. The company's vision is to bring deep learning to customers' data wherever it may be—from the edge to the datacenter—helping accelerate time-to-insight. Wave is powering the next generation of AI by combining its dataflow architecture with its MIPS embedded RISC multithreaded CPU cores and IP. Wave Computing has been named Frost & Sullivan's 2018 "Machine Learning Industry Technology Innovation Leader," and recognized by CIO Application Magazine's as one of the "Top 25 Artificial Intelligence Providers." Combined with MIPS, Wave now has over 400 granted and pending patents and hundreds of customers worldwide.