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MIPS M-Class M51xx Core Family

The MIPS M5150/M5100 processor cores are ideal for IoT, wearable and other embedded and real-time applications.

The M51xx cores are superset extensions of the MIPS microAptiv family, featuring:

- A five stage pipeline architecture delivering class-leading performance
- The microMIPS code size reduction ISA
- The MIPS DSP r2 module
- Fast interrupt handling
- Advanced debug/profiling capabilities
- Comprehensive power management

The M51xx cores implement the MIPS Release 5 architecture which incorporates hardware virtualization. Virtualization provides a foundation for MIPS multi-domain security that leads to the highest level of security of any embedded microcontroller architecture. Virtualization also enhances IP protection and reliability for a wide range of applications including: industrial controllers, Internet of Things (IoT), wearables, wireless communications, automotive and storage.

Virtualization support is provided for both the M5100 microcontroller-class and M5150 embedded processor versions of the M51xx family, a feature not available in competing alternatives.

Additional security is provided by the 'anti-tamper' feature in these cores, which includes countermeasures that provide resistance to unwanted access to the processor.

An optional IEEE 754 Floating Point Unit provides high-performance support of both single and double precision instructions.

Applications

- Industrial control and automation
- Internet of Things (IoT), Machine to Machine (M2M)
- Wearables
- Home appliances, digital consumer products
- Automotive
- Cloud computing
- Network communications
- Storage

Benefits

- Standard architecture, proven in millions of SoC designs
- High-performance, area- and energy- efficient architecture: performance requirement achieved at lower frequency and smaller size than the competition
- Hardware virtualization – supports multiple software environments running independently, securely, efficiently and in complete isolation to each other
- Available in microcontroller and embedded processor versions for use in a wide range of operating environments
- Combined MCU and DSP technology for cost-effective signal processing
- Flexibility and scalability – single design to cover a broad range of applications
- FPU to accelerate real-time control in industrial, automotive and digital consumer applications
- Broad software and ecosystem support, and mature toolchain
- Available as synthesizable IP for implementation in any process node, with standard cells and memories

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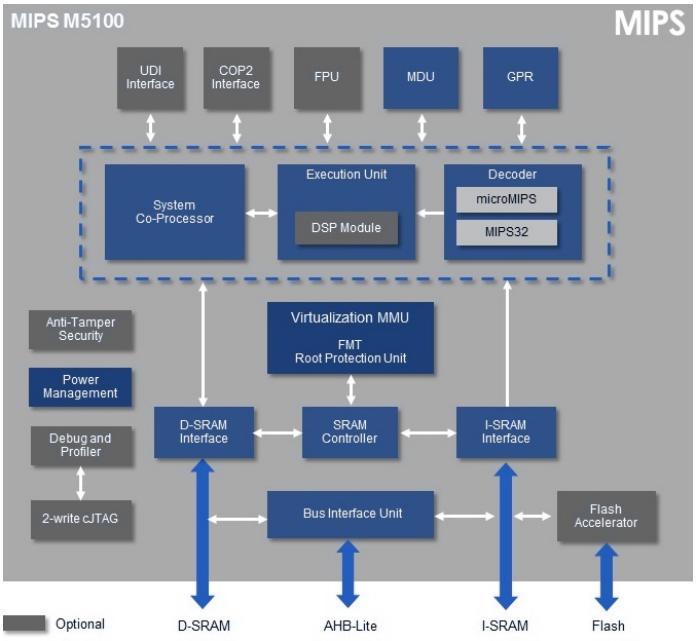
The M51xx family includes the following processor cores:

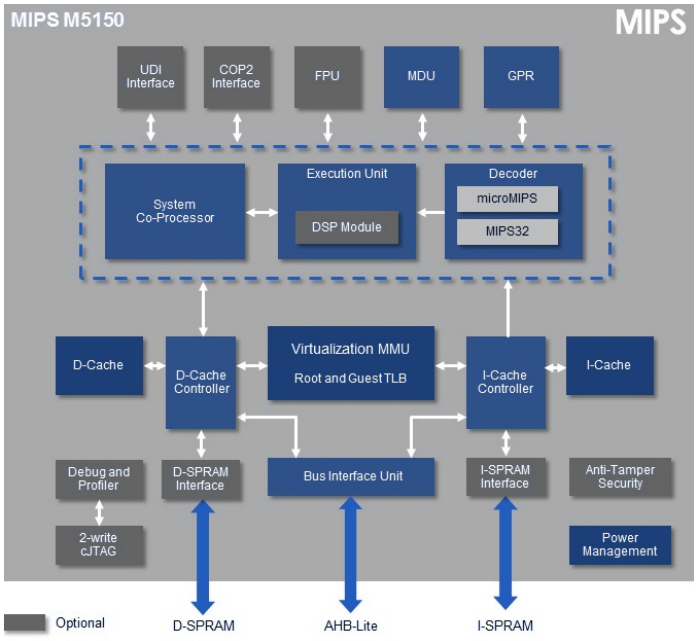
MIPS M5100

The MIPS M5100 features an integrated SRAM controller and a real time execution unit, optimized for low cost, low power microcontroller applications.



MIPS M5150

The MIPS M5150 incorporates a high performance L1 cache controller and virtual memory management support for high performance embedded system applications and rich operating systems.



MIPS Series5 Warrior M-class cores offer high performance, scalable and trusted solutions for a wide range of embedded applications.

The Warrior M-Class CPUs deliver class-leading performance and breakthrough hardware virtualization in the M5100 microcontroller class (MCU) and M5150 embedded processor cores.

The M51xx cores enable a broad range of systems to benefit from high levels of security, reliability and flexibility in a low-power, compact form factor.

The M51xx cores are enhancements of the MIPS microAptiv family designed with the same five-stage pipeline architecture, utilizing the high-performance digital signal processing (DSP) capabilities along with the microMIPS ISA for code size reduction.

Support is provided by a comprehensive set of hardware and software development tools from MIPS as well as a growing ecosystem of partners.

Several hypervisors for the M-Class cores are available and under development from MIPS and leading third party developers including Seltech and PUCRS University in Brazil.

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Architecture

- MIPS32 Release 5 Architecture
- microMIPS ISA
  - Enhanced code compression ISA of combined 16- and 32-bit instructions
  - Supports all existing MIPS32 instructions; adds new 16- and 32-bit instructions
  - Enables up to 30% code size reduction relative to 32-bit only code

Hardware Virtualization

- Create multiple execution environments (Guest) isolated from each other, operating at kernel privilege level
- Hypervisor/Secure Monitor (Root) manages access rights for each Guest
  - Supports Type 1 and Type II hypervisors
- Supports up to 7 Guests, each supplied a unique ID; Guest OS runs un-modified
- 7 new instructions facilitate Root-to-Guest communication
- Supports multiple Memory Management Unit options for optimum area vs. functionality
  - M5100 – FMT + Root Protection Unit
  - M5150 – Guest TLB + Root TLB
  - M5150 – Guest TLB + Root Protection Unit
- Allows sharing of resources (memory, DSP, FPU etc.) between Guests

DSP Module r2

- Dedicated pipeline, operates in parallel with core integer pipeline
- Implements over 150 instructions, including 70 SIMD and 38 Multiply/MAC instructions
- Enhanced Multiply & Divide Unit
  - Single cycle throughput multiply and MAC operations
  - Supports 32×32, 16×16, dual 16×16, dual 8×8, dual 8×16
- Supports up to 4 Accumulators

Floating Point Unit (FPU)

- Single and double precision IEEE 754 compliant FPU
- Supports IEEE-754 2008 Nan and ABS instructions
- Dedicated 7-stage pipeline, operating in parallel with core integer pipeline
- Most instructions execute with 1 cycle throughput and 4 cycle latency
- Executes 1:1 Core:FPU clock ratio
- Supports both MIPS32 and microMIPS instructions

Anti-Tamper

- Injection of random pipeline stalls
- Cache/SPRAM address and data scrambling
- 2 pseudo random number generators for use by the user software and core logic

Memory Controller

- M5150 – L1 cache controller for Instruction and Data sizes up to 64KB, 4-way set associative
- M5100 – 32-bit address and data SRAM interface, separate or unified instruction and data interface

Bus Interface Unit

- AMBA 3 AHB

EJTAG Debug & Trace

- Secure debug feature – prevents streaming instructions through the EJTAG port
- Supports enhanced iFlowtrace™ with additional event trace modes
- Simple/Complex instruction and data breakpoint support – 2I/1D, 4I/2D, 6I/2D, 8I/4D
- Support for 2 Performance Counters with multiple event type options
- Instruction and data address sampling: zero overhead, qualified read/write
- Support for 2-wire cJTAG debug interface

Power Management

- Incorporates extensive fine-grain clock gating
- Implements a Power Down mode initiated by a WAIT instruction

Expandability

- Optional co-processor (COP2) and CorExtend™ / User Defined Instruction (UDI) interfaces

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M5100 Core Specifications

Process Node	65LP		28HPM	
Optimization****	Speed	Area	Speed	Area
Frequency* (MHz)	322	100	497	100
Performance (DMIPS)	505	157	780	157
Area** (mm²)	0.77	0.2	0.23	0.04
Core Active Power*** (mW/MHz)	0.11	0.05	0.04	0.017
Sleep Power (µW/MHz)	5.8	2.3	1.7	0.8
Cell Library	9T LVt	9T SVt	12T SVt	9T LVt

M5150 Core Specifications

Process Node	65LP	28HPM
Optimization****	Speed	Speed
Frequency* (MHz)	372	576
Performance (DMIPS)	584	904
Area** (mm²)	0.89	0.26
Core Active Power*** (mW/MHz)	0.13	0.07
Sleep Power (µW/MHz)	2.7	1.5
Cell Library	9T LVt	12T SVt

Notes: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process

* Production frequency PTSI
65LP: +/- 5% OCV, 50ps clock jitter
28HPM: +/- 4% OCV, 25ps clock jitter

** Core Floorplanned area
*** Power measured at typical corner, 25C at 1.2V/65LP, 0.9V/28HPM
**** M5100 Speed Optimized – microMIPS + FPU + DSP + 32KB/32KB I/D SRAM, FMT+32RPU + AHB
**** M5100 Area Optimized – microMIPS + DSP +8RPU
Area optimized frequency can be higher/lower than the target chosen
**** M5150 Speed Optimized – microMIPS + FPU + DSP + 32KB/32KB I$/D$ + 32RTLB/32GTLB + AHB

About Wave Computing
Wave Computing, Inc. is revolutionizing AI with its dataflow-based systems and solutions that deliver orders of magnitude performance improvements over legacy architectures. The company's vision is to bring deep learning to customers' data wherever it may be—from the edge to the datacenter—helping accelerate time-to-insight. Wave is powering the next generation of AI by combining its dataflow architecture with its MIPS embedded RISC multithreaded CPU cores and IP. Wave Computing has been named Frost & Sullivan's 2018 "Machine Learning Industry Technology Innovation Leader," and recognized by CIO Application Magazine's as one of the "Top 25 Artificial Intelligence Providers." Combined with MIPS, Wave now has over 400 granted and pending patents and hundreds of customers worldwide.