300 Orchard City Dr, Suite #170
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MIPS M-Class M62xx Processor Cores

The MIPS M6200/M6250 processor cores are ideal for microcontroller and embedded-type applications. The M62xx cores are superset extensions of the MIPS microAptiv family, being the first M-Class processors to implement the latest MIPS Release 6 Architecture. The M6200 and M6250 implement a 6-stage pipeline design and continue to support both MIPS32 and microMIPS ISAs.

These new processor cores continue the M-Class line-up in offering both a microcontroller (MCU) and microprocessor (MPU) versions within the same family. The M6200 and M6250 continue the evolution of the M-Class processors, offering improved performance and additional features from the microAptiv cores.

Applications

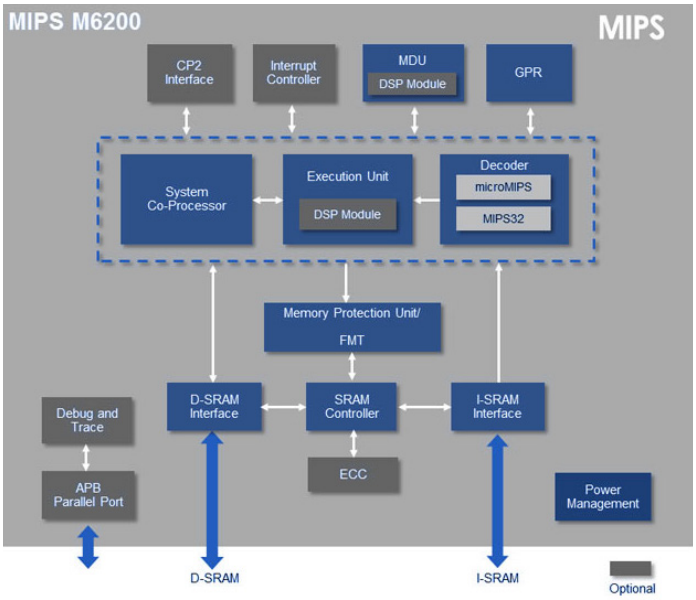
These cores provide a compelling solution for a wider range of applications requiring high operating frequency, increased memory throughout, data integrity support in a low power, small area footprint including:

- Internet of Things (IoT) and Machine to Machine (M2M) devices
- High frequency networks, packet inspection/messaging processing systems
- Large address space embedded applications – SSD and flash controllers, GPU co-processors
- High reliability industrial, enterprise, and automotive systems
- Wearables

The M62xx family includes the following processor cores:

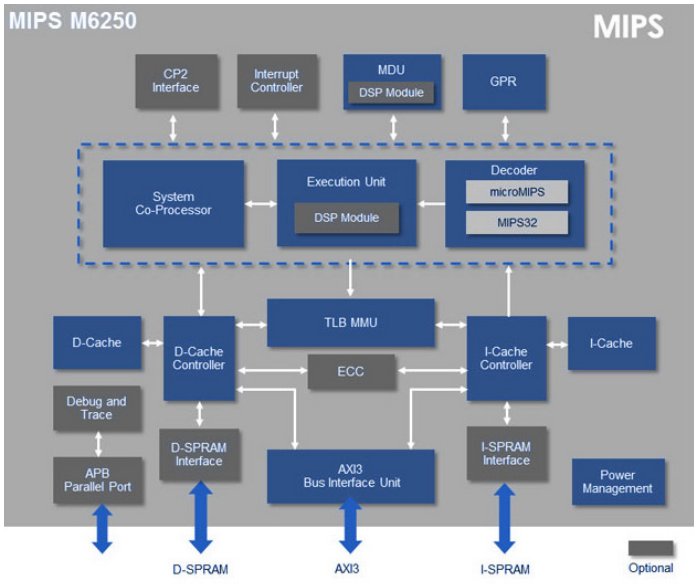
MIPS M6200

The MIPS M6200 features an integrated 64-bit SRAM controller, a memory protection unit, and a real-time, low-latency execution unit, optimized for cost-efficient, low-power microcontroller and embedded applications.



MIPS M6250

The MIPS M6250 incorporates a high-performance instruction/data L1 cache controller and a Memory Management Unit (MMU), enabling execution of Linux and other rich operating systems for high performance embedded applications.



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Key features

- 30% higher frequency of equivalent MIPS microAptiv implementations
- 6 stage pipeline
  - Load/Store architecture with single cycle ALU operations
- Dedicated DSP and SIMD module
  - Single cycle throughput multiply and MAC operations
  - Supports 32×32, 16×16, dual 16×16, dual 8×8, dual 8×16
  - Implements over 150 instructions, including 70 SIMD and 38 Multiply/MAC instructions
  - Supports up to 4 Accumulators
- 32 General Purpose Registers
  - Up to 16 shadow register sets
- M6200: Tightly coupled SRAM controller
  - Single cycle
  - 32-bit address, 64-bit data
  - Dual instruction and data interfaces
- M6250: Programmable L1 instruction/data cache controller
  - Up to 64KB, 2 or 4-Way Set Associative
  - 64-byte cache line size
  - 64-bit instruction/data cache, accessible in same pipeline cycle
- M6250: Optional Tightly Coupled Sratchpad RAM (SPRAM) controller
  - Up to 1MB instruction/data SPRAM
- Data Integrity: Error Correction (ECC) and parity
  - ECC support on instruction and data memories: SPRAM, L1 cache and SPRAM
  - Single error correction and double error detection (SECDED)
  - Parity support on instruction and data
- Up to 4GB Virtual Memory support – User, Kernel and Debug modes
- M6200 Memory Management Unit (MMU)
  - Up to 16 region Memory Protection Unit with address, size and protection options
  - Fixed Memory Translation (FMT)
- M6250 Memory Management Unit (MMU)
  - Instruction/Data Translation Lookaside Bufer (TLB)
  - 32/dual entry 16 fully associative Joint TLB (JTLB)
  - 4-entry Instruction TLB and 4-entry Data TLB
- M6250: 40-bit eXtended Physical Addressing
- MCU Application Specific Extension (MCU ASE)
  - Supports up to 255 interrupts from external interrupt controller
  - Separate priority and vector generation
  - Automated interrupt handling instructions
  - Supports tailchaining
  - Supports use of GPR shadow sets for reduced interrupt latency
- Interrupt Control Unit (optional)
  - Supports up to 255 configurable interrupts
  - Supports interrupt source sensitivity (level-positive, level-negative, edge-positive, edge-negative, dual-edge-sensitive)
- Debug Port
  - AMBA APB parallel debug port
  - Supports mixed-core debugging
- MIPS Debug Hub (optional)
  - Supports connections to JTAG and/or APB compatible debug systems
  - Supports multi-core debugging
- Debug and Trace profiling
  - Simple instruction/data breakpoint support – 4I/2D, 8I/4D
  - Complex instruction/data breakpoint support – 8I/4D
  - Fast Debug Channel
  - Performance Counters and PC/Address Sampling profiling support
  - iFlowtrace Instruction Trace
- Secure Debug
- M6250: AMBA 3 AXI Bus Interface Unit
- Power Management
  - Incorporates extensive fine-grain clock gating
  - Power Down modes initiated by a register control or WAIT instruction

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28HPM 12T SVt	M6200	M6250
Freq (MHz)	750	750
Core Area (mm²)	0.19	0.23
Core Power (µW/MHz)	60	62

DSP enabled, 16-region Memory Protection Unit (M6200), 32 entry JTLB (M6250)
Frequency measured at slow corner, 0.81V, 0C, OCV, +/-5%, 25ps clock jitter
Core area is floorplanned, pre-shrunk
Core power measured at typical corner, 0.9V, 25C

About Wave Computing
Wave Computing, Inc. is revolutionizing AI with its dataflow-based systems and solutions that deliver orders of magnitude performance improvements over legacy architectures. The company's vision is to bring deep learning to customers' data wherever it may be—from the edge to the datacenter—helping accelerate time-to-insight. Wave is powering the next generation of AI by combining its dataflow architecture with its MIPS embedded RISC multithreaded CPU cores and IP. Wave Computing has been named Frost & Sullivan's 2018 "Machine Learning Industry Technology Innovation Leader," and recognized by CIO Application Magazine's as one of the "Top 25 Artificial Intelligence Providers." Combined with MIPS, Wave now has over 400 granted and pending patents and hundreds of customers worldwide.