300 Orchard City Dr, Suite #170
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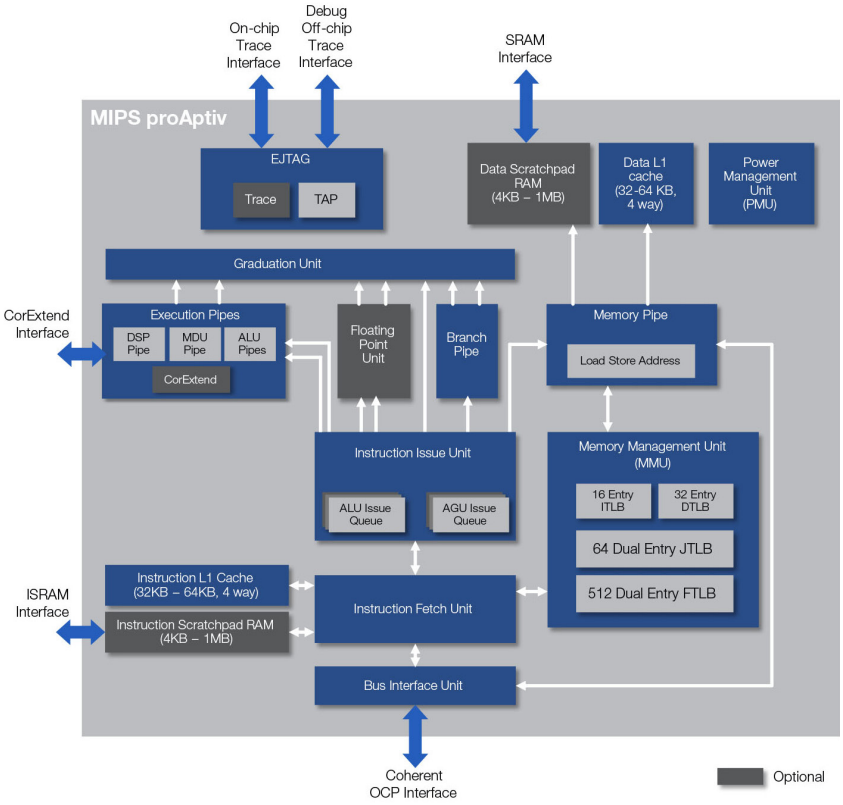
MIPS proAptiv Processor Core

MIPS proAptiv is a family of microprocessor IP cores designed to deliver the compelling top-line performance required for connected consumer electronics including connected TVs and set-top boxes and high-performance compute in embedded applications.

proAptiv CPUs are based on a wide issue, deeply out-of-order (OoO) implementation of the MIPS32 architecture, and are available in single and multi-core product versions supporting up to six cores.

The proAptiv family leverages an advanced microarchitecture, an upgraded floating point unit (FPU), and an enhanced multi-core interconnect to deliver a major leap forward in performance over the previous generation of MIPS Classic CPU IP cores, while implementing in nearly the half the size of competing cores in the same process node.



Features

- 32-bit MIPS32® Release 3 Instruction Set Architecture with up to six cores
- High-performance, 16-stage, multiissue out-of-order (OoO) pipeline
- I/D L1 cache sizes of 32KB or 64KB each, 4-way set associative
- Programmable Memory Management Unit (MMU)
- MIPS DSP Module, version 2
- Optional 2nd gen hi-performance dual-issue Floating Point Unit (FPU)
- Advanced power management at base core and multi-core cluster levels
- EJTAG/PDtrace debug

Benefits

- Superscalar, OoO processor available in application-optimized single and multicore versions
- Sophisticated branch prediction for performance on modern software workloads
- Load/Store bonding for optimum data movement performance
- EVA (Enhanced Virtual Addressing) – programmable virtual address map for optimal use of 32-bit address space
- Industry leading benchmark and real world performance without an increase in area and power
- Broad software and ecosystem support and mature toolchain
- Available as synthesizable IP, for implementation in any process node, with standard cells and memories

Applications

- Connected DTV/STB
- Networking
- Automotive infotainment
- High-performance compute

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Baseline Specifications

Target Specifications	TSMC 28HPM
Frequency	1 GHz - 2+ GHz*
CoreMark/MHz (per core)	5.1
Total CoreMark @ 1.5 GHz	> 7500 per core
DMIPS/MHz (per core)	3.5
Total DMIPS @ 1.5 GHz	> 5250 per core

Notes: Frequencies indicated are for fully floorplanned dual core implementation, ranging from 12T SVt area-optimized in worst case silicon corner, to 12T MVt speed-optimized typical corner silicon.

Each base core configuration:

- 32KB Data/Inst L1 caches with parity, BIST
- New high-speed FPU
- Fully-featured MMU, using multi-level TLB (I/D uTLBs + 128 entry VTLB + 1024 entry FTLB)
- PDtrace™ debug

Multi-core cluster configuration:

- Dual fully-configured proAptiv cores per above
- Coherence Manager + integrated 1MB L2$ w/ECC
- One hardware IO Coherence Unit (IOCU) port

Cluster level PDtrace Implementation libraries/parameters – speed optimized, based on:

- TSMC 28HPM 12T standard cells + Synopsys memories
- Worst case, slow-slow corner silicon (zero temp, WCZ) with 10% OCV + 25ps clock jitter margins, except where noted at typical silicon.

About Wave Computing

Wave Computing, Inc. is revolutionizing AI with its dataflow-based systems and solutions that deliver orders of magnitude performance improvements over legacy architectures. The company's vision is to bring deep learning to customers' data wherever it may be—from the edge to the datacenter—helping accelerate time-to-insight. Wave is powering the next generation of AI by combining its dataflow architecture with its MIPS embedded RISC multithreaded CPU cores and IP. Wave Computing has been named Frost & Sullivan's 2018 "Machine Learning Industry Technology Innovation Leader," and recognized by CIO Application Magazine's as one of the "Top 25 Artificial Intelligence Providers." Combined with MIPS, Wave now has over 400 granted and pending patents and hundreds of customers worldwide.